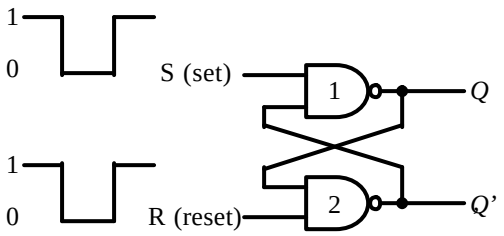
TEKNIK DIGITAL (A)
(TI 2104)

Materi Kuliah ke-7

FLIP-FLOPS

Basic RS Flip-Flop (NAND)



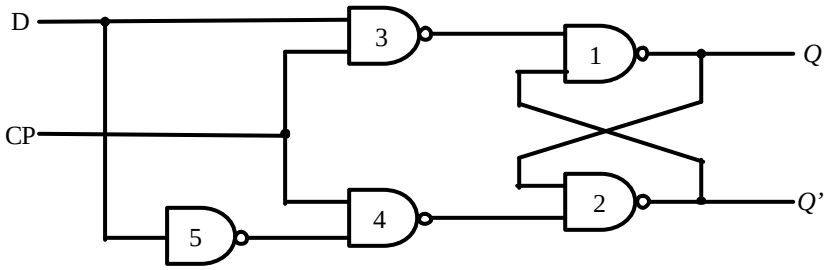
(a) Logic diagram

S	*R*	*Q*	*Q'*	
1	0	0	1	
1	1	0	1	(after S = 1, R = 0)
0	1	1	0	
1	1	1	0	(after S = 0, R = 1)
0	0	1	1	

(b) Truth table

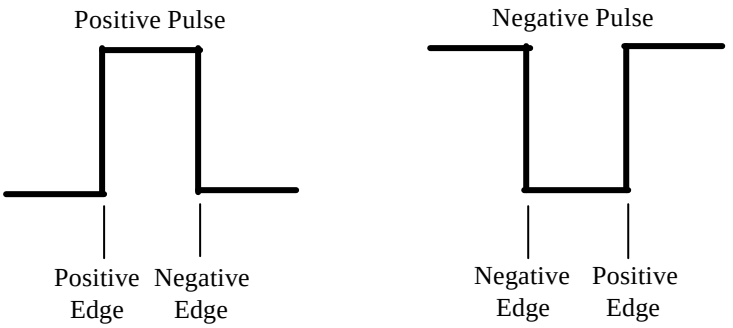
A flip-flop holds 1 "bit".
"Bit" ::= "binary digit."

Clocked D Flip-Flop



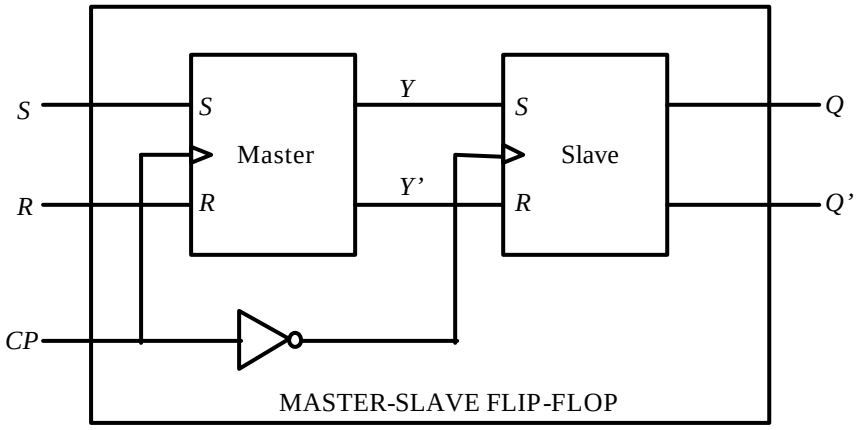
The present state is held when CP is low.

Clock Pulse Definition

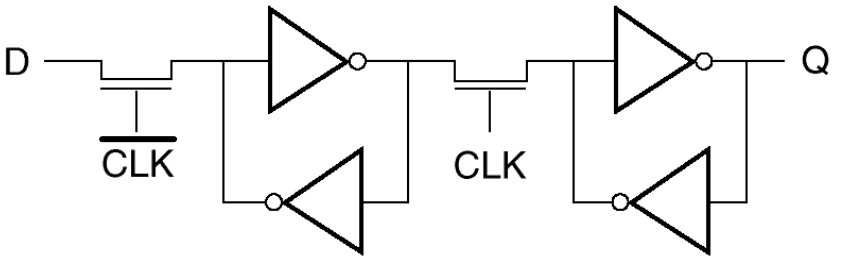


Edges can also be referred to as leading and trailing.

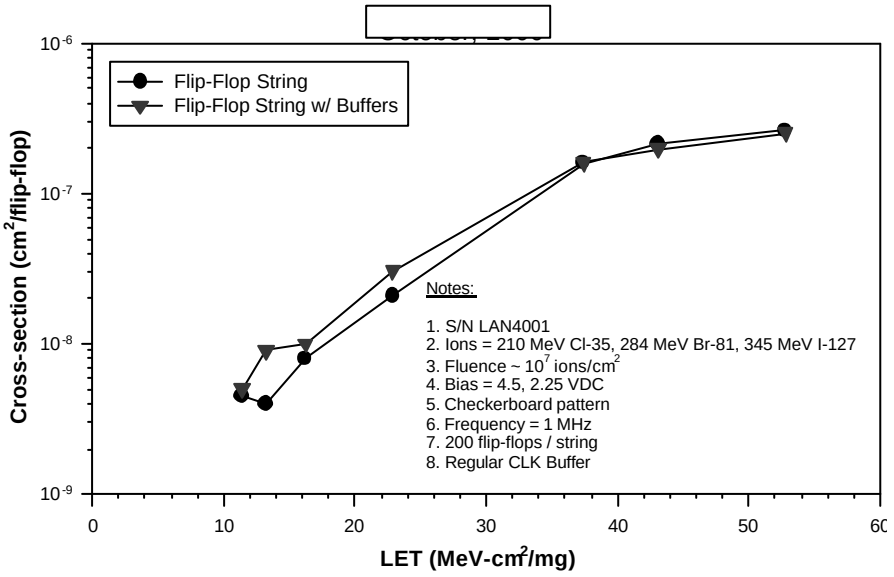
Master-Slave Flip-Flop



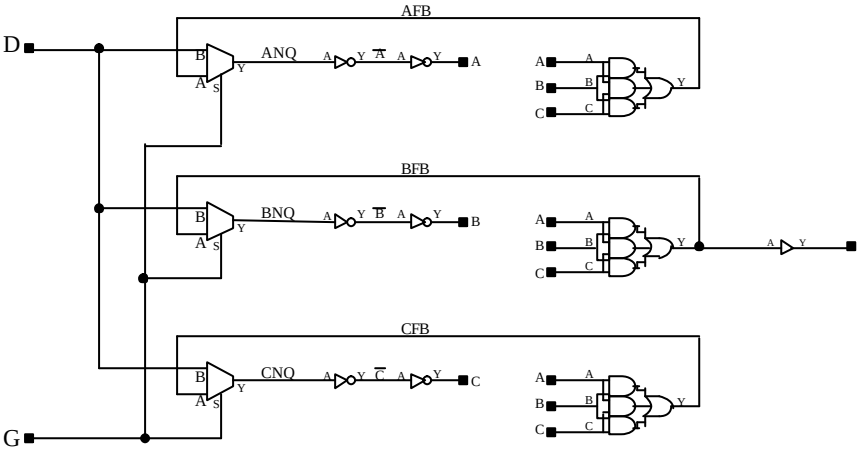
Flip-Flop on RT54SX-A (Not hardened)



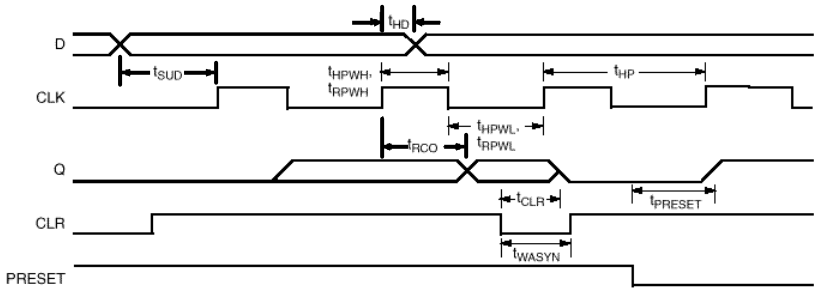
RT54SX-A SEU Performance



RT54SX-S Latch (SEU Hardened)



Flip-Flop Timing: RT54SX-S



Worst-case Military Conditions, V_{CCA}=2.3, V_{CCI}=3.0V, T_J=125°C
-1 Speed Grade

		Min	Max	Units
t_{RCO}	Sequential Clock-to-Q		1.0	ns
t_{CLR}	Asynchronous Clear-to-Q		0.9	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.6		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.8		ns

Metastability - Introduction

- Can occur if the setup, hold time, or clock pulse width of a flip-flop is not met.
- A problem for asynchronous systems or events.
- Can be a problem in synchronous systems.
- Three possible symptoms:
  - Increased CLK -> Q delay.
  - Output a non-logic level
  - Output switching and then returning to its original state.
- Theoretically, the amount of time a device stays in the metastable state may be infinite.
- Many designers are not aware of metastability.

Metastability

- In practical circuits, there is sufficient noise to move the device output of the metastable state and into one of the two legal ones. This time can not be bound. It is statistical.
- Factors that affect a flip-flop's metastable "performance" include the circuit design and the process the device is fabricated on.
- The resolution time is not linear with increased circuit time and the MTBF is an exponential function of the available slack time.

Metastability - Calculation

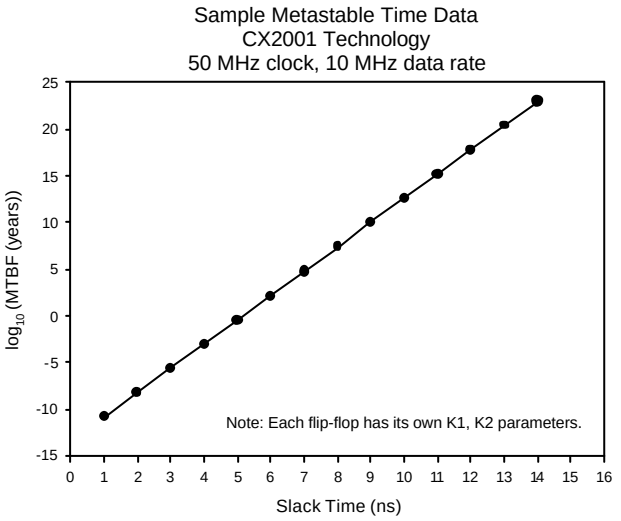
- $MTBF = e^{K2*t} / (K1 \times F_{CLK} \times F_{DATA})$

  t is the slack time available for settling

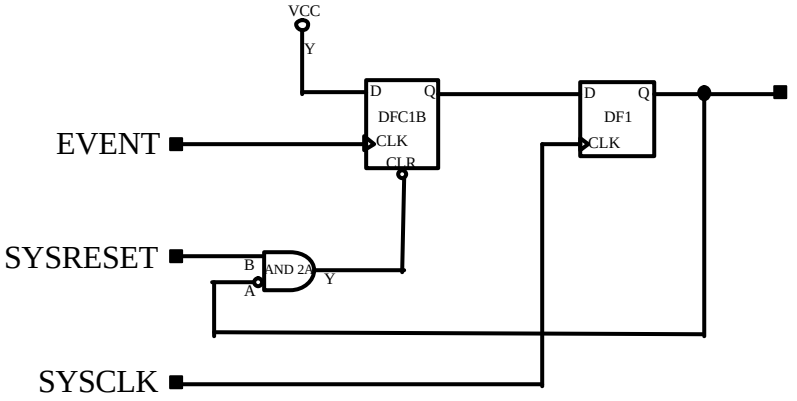
  K1 and K2 are constants that are characteristic of the flip-flop

  Fclock and Fdata are the frequency of the synchronizing clock and asynchronous data.
- Software is available to automate the calculations with built-in tables of parameters.
- Not all manufacturers provide data.

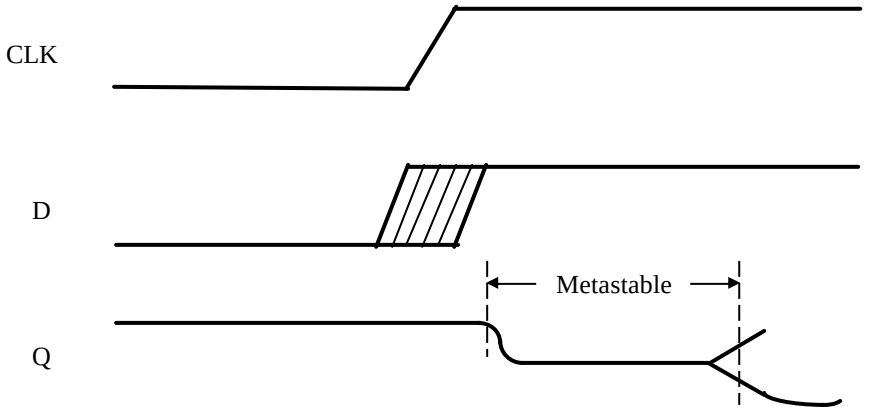
Metastability - Sample Data



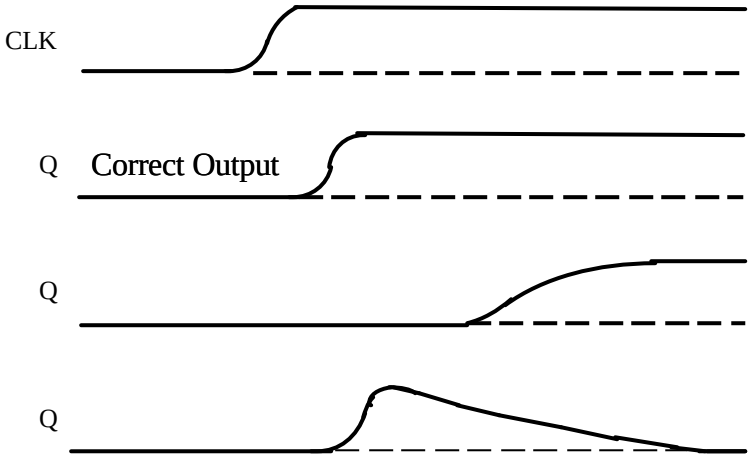
Synchronizer (Bad Circuit)



Metastable State: Possible Output from a Flip-flop

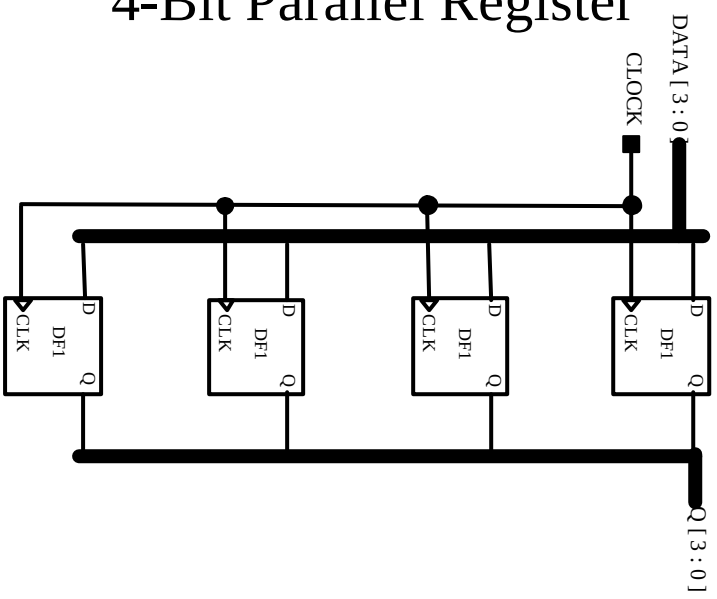


Metastable State: Possible Outputs from a Flip-flop

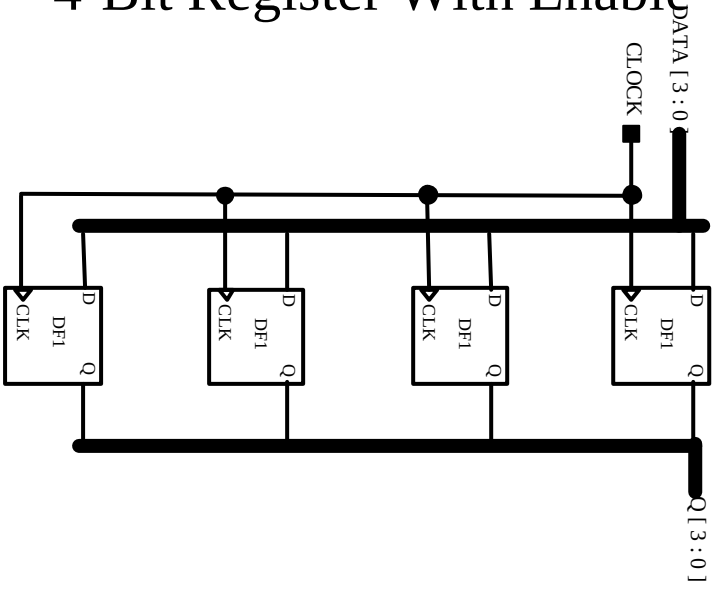


Parallel Registers

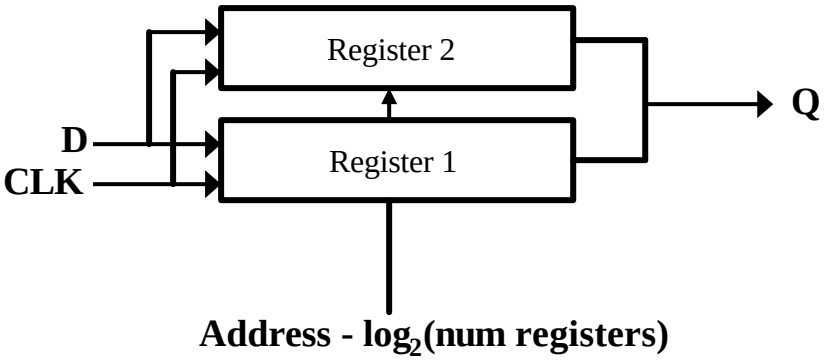
4-Bit Parallel Register



4-Bit Register With Enable



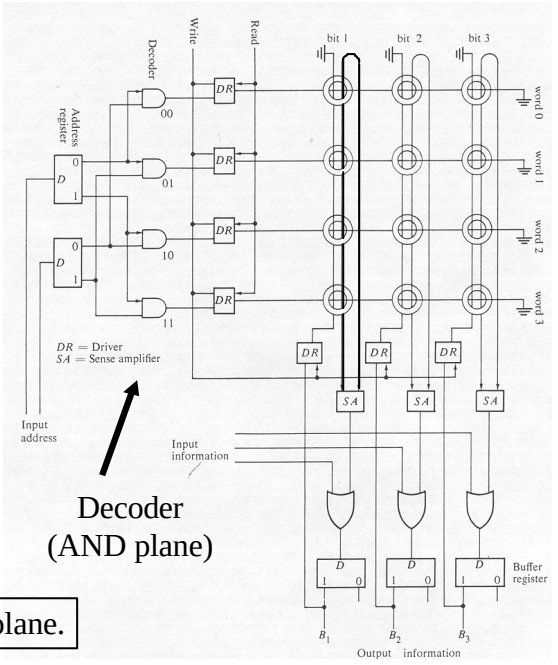
Register Files (Simplified)



D and Q are both sets of lines, with the number of lines equal to the width of each register. There are often multiple address ports, as well as additional data ports.

Memory Devices

Magnetic Core Memory

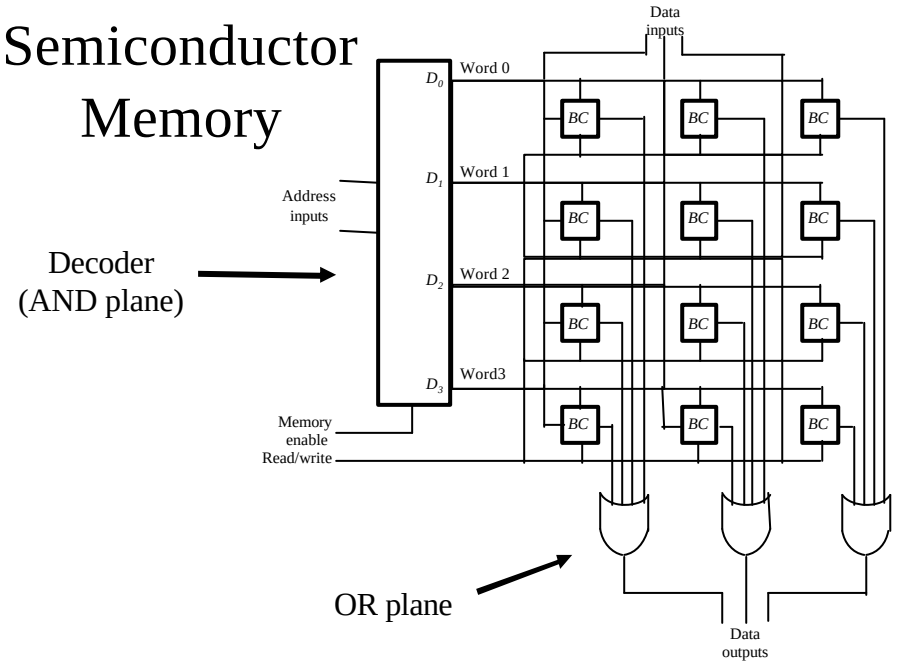


Register

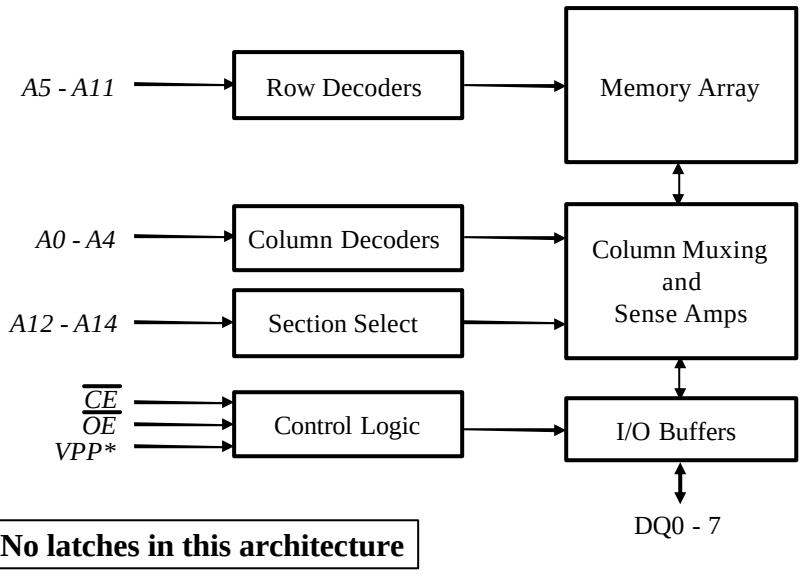
Decoder (AND plane)

Sense wires serve as OR plane.

Semiconductor Memory



Rad-Hard PROM Architecture



No latches in this architecture

W28C64 EEPROM

Simplified Block Diagram